UNITED STATES DEPARTMENT OF COMMERCE
United States Patent and Trademark Office
Address: COMMISSIONER FOR PATENTS
P O Box 1450
Alexandria, Virginia 22313-1450
www uspto gov

APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
10/713,563	11/13/2003	Robert M. Ellis	5038-298	8266

32231 7590 05/08/2009
MARGER JOHNSON & MCCOLLOM, P.C. - Intel
210 SW MORRISON STREET, SUITE 400
PORTLAND, OR 97204

EXAMINER	
KROFCHECK, MICHAEL C	
ART UNIT	**PAPER NUMBER**
2186	
MAIL DATE	**DELIVERY MODE**
05/08/2009	PAPER

Please find below and/or attached an Office communication concerning this application or proceeding.

The time period for reply, if any, is set in the attached communication.

Office Action Summary	Application No.	Applicant(s)	
	10/713,563	ELLIS, ROBERT M.	
	Examiner	Art Unit	
	MICHAEL C. KROFCHECK	2186	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE *3* MONTH(S) OR THIRTY (30) DAYS, WHICHEVER IS LONGER, FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *05 February 2009*.

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1-17 and 22-26* is/are pending in the application.

4a) Of the above claim(s) *16,17 and 22-24* is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1-15,25 and 26* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☒ The drawing(s) filed on *27 October 2006* is/are: a)☒ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)

2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)

3) ☐ Information Disclosure Statement(s) (PTO/SB/08) Paper No(s)/Mail Date _____.

4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____ .

5) ☐ Notice of Informal Patent Application

6) ☐ Other: _____.

DETAILED ACTION

1. In view of the appeal brief filed on 2/5/2009, PROSECUTION IS HEREBY REOPENED. New grounds of rejection are set forth below.

To avoid abandonment of the application, appellant must exercise one of the following two options:

(1) file a reply under 37 CFR 1.111 (if this Office action is non-final) or a reply under 37 CFR 1.113 (if this Office action is final); or,

(2) initiate a new appeal by filing a notice of appeal under 37 CFR 41.31 followed by an appeal brief under 37 CFR 41.37. The previously paid notice of appeal fee and appeal brief fee can be applied to the new appeal. If, however, the appeal fees set forth in 37 CFR 41.20 have been increased since they were previously paid, then appellant must pay the difference between the increased fees and the amount previously paid.

Claim Objections

2. Claim 15 is objected to under 37 CFR 1.75(c), as being of improper dependent form for failing to further limit the subject matter of a previous claim. Applicant is required to cancel the claim(s), or amend the claim(s) to place the claim(s) in proper dependent form, or rewrite the claim(s) in independent form.

3. Claim 15 is directed to an article machine-readable code embodied on a medium that when executed causes the machine to transmit a synchronization signal on the data lane if the measured data transition number is less than the desired data transition number. This specific limitation is recited in the exact same manner in parent claim 14.

Claim Rejections - 35 USC § 103

4. The factual inquiries set forth in *Graham* **v.** *John Deere Co.*, 383 U.S. 1, 148 USPQ 459 (1966), that are applied for establishing a background for determining obviousness under 35 U.S.C. 103(a) are summarized as follows:

1. Determining the scope and contents of the prior art.
2. Ascertaining the differences between the prior art and the claims at issue.
3. Resolving the level of ordinary skill in the pertinent art.
4. Considering objective evidence present in the application indicating obviousness or nonobviousness.

5. Claims 1-9, 11-12, 14-15, 25-26 are rejected under 35 U.S.C. 103(a) as being unpatentable over Polzin et al. (US 2004/0230718) and Boggs et al. (US 5,530,696).

6. With respect to claim 1, Polzin teaches of a method comprising at least one data lane in a point to point memory channel having a plurality of data lanes (fig. 1; paragraph 24).

Polzin fails to explicitly teach of calculating an achieved data transition density for at least one data lane, the achieved data transition density calculated over greater than two clock cycles.

However, Boggs teaches of calculating an achieved data transition density for at least one data lane, the achieved data transition density calculated over greater than two clock cycles (fig. 2; column 6, lines 15-24).

The combination of Polzin and Boggs teaches of transmitting a synchronization on the at least one data lane responsive to the achieved transition density (Polzin,

paragraph 40; where when more transitions are needed for the transmission density to be sufficient, the data on each bit is scrambled to achieve the additional transitions).

It would have been obvious to one of ordinary skill in the art having the teachings of Polzin and Boggs at the time of the invention to include the clock and transition counters of Boggs in Polzin. Their motivation would have been to determine exactly when the transmission density is lacking, and scrambling of the data is needed.

7. With respect to claim 5, Polzin teaches of a memory channel comprising: a host and a plurality of DIMMs connected in a point-to-point fashion, wherein the host includes a processor (fig. 1; paragraph 24-25);

an outbound data channel and an inbound data channel, each having a plurality of data lanes (fig. 1; paragraph 24);

a transition generator configured to transmit a synchronization signal on the at least one data lane if the achieved transition density is less than the desired data transition density (paragraph 40).

Boggs teaches of wherein the achieved transition density is measured over greater than two clock cycles (fig. 2; column 6, lines 15-21).

The combination of Polzin and Boggs teaches of at least one transition detection circuit configured to detect whether an achieved data transition density on at least one data lane is less than a desired data transition density for the at least one data lane (Boggs, fig. 2; column 6, lines 22-24; Polzin, paragraph 40; as in the combination, the sufficient number of data transitions are needed for phase alignment, it is clear that it

can be determined when the number of transitions are insufficient in order for Polzin's scrambling to be carried out).

With respect to claims 14 and 15, Polzin teaches of an article of machine-readable code, embodied on a machine- readable medium, that when executed causes a machine to perform processes (paragraph 4-5, as the memory access and controlling occurs in a computer system, it is abundantly clear to one of ordinary skill in the art that there is a memory storing the instructions required for the controllers to carry out their functions) comprising: storing a desired data transition number (paragraph 40);

a data lane in a point-to-point memory channel (fig. 1; paragraph 24).

Boggs teaches of storing a clock cycle number that is greater than two (fig. 2; column 6, lines 15-18);

The combination of Polzin and Boggs teaches of for a data lane in a point-to-point memory channel, recording a measured data transition number over a period of clock cycles equal to the clock cycle number (Boggs, column 6, lines 22-24 and 41-52);

comparing the measured data transition number to the desired data transition number (Polzin, paragraph 40; as in the combination, the sufficient number of data transitions are needed for phase alignment, it is clear that it must be determined when the number of transitions are insufficient in order for Polzin's scrambling to be carried out, this would be carried out by a comparison of the transitions counted with Boggs counter and the sufficient number of Polzin); and

transmitting a synchronization signal on the data lane if the measured data transition number is less than the desired data transition number (Polzin, paragraph 40).

8. With respect to claim 2, Boggs teaches of wherein calculating an achieved data transition density for the at least one data lane comprises: counting how many times a data transition occurs on the at least one data lane during a predetermined number of clock cycles, the predetermined number of clock cycles being greater than two (fig. 2; column 6, lines 15-24).

9. With respect to claim 3, the combination of Polzin and Boggs teaches of the limitations cited as described above with respect to claim 14.

10. With respect to claim 4, Polzin teaches of wherein transmitting a synchronization signal on the at least one data lane responsive to the achieved transition density comprises: transmitting a synchronization signal on all the data lanes if the achieved data transition density is less than the desired data transition density on the at least one data lane (paragraph 40).

11. With respect to claim 6, the combination of Polzin and Boggs teaches of wherein the at least one transition detection circuit is located on the host (Polzin, fig. 1, 3; paragraph 40-41, as the data recovery unit recovers the scrambled data bit, the transition detecting (from Boggs) and scrambling would have had to occur upstream of the downlink, thus in the originating host).

12. With respect to claim 7, the combination of Polzin and Boggs teaches of wherein the at least one transition detection circuit is located on a corresponding one of the plurality of DIMMs (Polzin fig. 1, 3-4; paragraph 40-41, 52; as the transmit unit scrambles outgoing data, the transition detecting of Boggs is also located there to control when the scrambling occurs).

13. With respect to claim 8, Boggs teaches of wherein the at least one transition detection circuit comprises: a plurality of data transition detectors, each configured to detect a data transition on a corresponding data lane (fig. 2; column 6, lines 22-24; in the combination, there is a detector corresponding to each bit line of Polkin as data is scrambled on a bit line basis (Polzin, paragraph 40));

a clock cycle counter (fig. 2; column 5, lines 51-60);

a plurality of data transition counters, each configured to count the data transitions detected by a corresponding data transition detector, and configured to be reset by the clock cycle counter (fig. 2; column 6, lines 22-24 and 41-46);

The combination of Polzin and Boggs teaches of a logic block configured to signal when at least one of the plurality of data transition counters counts, during a time period defined by the clock cycle counter, a number of data transitions detected by the corresponding data transition detector that is less than the desired data transition density (Polzin; paragraph 40 as the data bits are scrambled when the transition number is insufficient, it is clear that there is an object that signals to the scrambler to scramble the data bits).

14. With respect to claim 11, the combination of Polzin and Boggs teaches of the limitations cited and described above with respect to claim 8. The combination of Polzin and Boggs also teaches of a first logic block configured to signal when at least one of the plurality of data transition counters corresponding to the data lanes on the outbound data path counts, during a time period defined by the clock cycle counter, a number of data transitions detected by the corresponding data transition detector that is less than

the desired data transition density (Polzin; paragraph 40 as the data bits are scrambled when the transition number is insufficient, it is clear that there is an object that signals to the scrambler to scramble the data bits); and

a second logic block configured to signal when at least one of the plurality of data transition counters corresponding to the data lanes on the inbound data path counts, during a time period defined by the clock cycle counter, a number of data transitions detected by the corresponding data transition detector that is less than the desired data transition density (Polzin; paragraph 40, 52 as the data bits are scrambled when the transition number is insufficient, it is clear that there is an object that signals to the scrambler to scramble the data bits);

15. With respect to claims 9 and 12, Boggs teaches of wherein the clock cycle counter and the plurality of data transition counters are programmable (fig. 2; column 5, lines 51-61, column 6, lines 15-32).

16. With respect to claim 25, Polzin teaches of wherein transmitting the synchronization signal on the at least one data lane comprises: transmitting the synchronization signal having a number of transitions to cause the achieved data transition density for the at least one data lane to the greater than or equal to a desired data transition density (paragraph 40).

17. With respect to claim 26, the combination of Polzin and Boggs teaches of the transition detection circuit is configured to detect whether an achieved data transition density on a corresponding one of the at least one data lane is less than the desired data transition density for the corresponding data lane (Boggs, fig. 2; column 6, lines 22-

24; Polzin, paragraph 40; as in the combination, the sufficient number of data transitions are needed for phase alignment, it is clear that it can be determined when the number of transitions are insufficient in order for Polzin's scrambling to be carried out).

18. Claims 10 and 13 are rejected under 35 U.S.C. 103(a) as being unpatentable over Polzin and Boggs as applied to claims 8 and 11 respectively, and further in view of the applicant's admitted prior art (AAPA).

19. With respect to claims 10 and 13, the combination of Polzin and Boggs fails to explicitly teach of wherein the logic block comprises an AND gate and a plurality of NAND gates.

However, AAPA teaches of wherein the logic block comprises an AND gate and a plurality of NAND gates (specification page 4, lines 18-21, 25-27).

It would have been obvious to one of ordinary skill in the art having the teachings of Polzin, Boggs, and AAPA at the time of the invention to use the NAND and AND gates of AAPA in the combination of Polzin and Boggs as those of ordinary skill in the art are familiar with using the NAND and AND gates to create output signals (AAPA, page 4, lines 19-21, 25-27) such as the control signal of Bashirullah.

Response to Arguments

20. Applicant's arguments, see section B, pages 7-10 of the appeal brief, filed 2/5/2009, with respect to the rejection(s) of claim(s) 1, 5, and 14 under 35 USC 103(a) have been fully considered and are persuasive. Therefore, the rejection has been

withdrawn. However, upon further consideration, a new ground(s) of rejection is made in view of Polzin et al. (US 2004/0230718).

Conclusion

21. A Supervisory Patent Examiner (SPE) has approved of reopening prosecution by signing below.

22. Any inquiry concerning this communication or earlier communications from the examiner should be directed to Michael Krofcheck whose telephone number is 571-272-8193. The examiner can normally be reached on Monday - Friday.

23. If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Matt Kim can be reached on 571-272-4182. The fax phone number for the organization where this application or proceeding is assigned is 571-273-8300.

24. Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free).

/MICHAEL C KROFCHECK/
Examiner, Art Unit 2186

/Matt Kim/

Supervisory Patent Examiner, Art Unit 2186

Michael Krofcheck